Claims:

1. A computer, comprising:

data registers for storing uncompressed data;

a data queue for storing data to be compressed;

a compressor for compressing data in said data queue;

a compression ratio monitor for determining the compression ratio of compressed data;

a compression control register for holding control information; and

a precision reducer for reducing the precision of data in said data registers and for storing reduced precision data in said data queue;

wherein said precision reducer operates in response to control information;

wherein said precision reducer reduces the precision of data such that the resulting reduced precision data can be more efficiently compressed by said compressor; and

wherein said control information depends on said compression ratio monitor.

2. The computer of claim 1, further including a compressed memory for storing compressed data.

3. The computer of claim 2, wherein said control information causes said precision reducer to operate when said compressed memory is near full.

4. The computer of claim 1, wherein said precision reducer reduces precision by truncating data by reducing bits to zero.

5. The computer of claim 4, wherein said precision reducer scales data by shifting data to prior to truncating.

6. The computer of claim 1, wherein said precision reducer converts floating point data to integer data by denormalizing the floating point data, wherein said floating point data includes a sign bit, an exponent component, and a fraction component.

7. The computer of claim 6, wherein said denormalizing is performed by shifting data the number of times represented by the exponent component.

8. The computer of claim 7, wherein said precision reducer truncates data when said floating point data represents a negative number.

9. The computer of claim 8, wherein said precision reducer truncates data by reducing bits to zero

10. The computer of claim 2, wherein said compression ratio monitor traps to a software program when said compression ratio drops below a predetermined value.

11. The computer of claim 10, wherein after said compression ratio monitor traps to said software program that software program checks the fill status of said compressed memory.

12. The computer of claim 11, wherein said software program modifies the compression control register such that control information causes said precision reducer to operate when said compressed memory is near full.

13. The computer of claim 12, wherein said software program is an operating system.

14. The computer of claim 12, further including a processor for running an application program.

15. The computer of claim 14, wherein said application program is a computer game.

16. The computer of claim 1, wherein said precision reducer operates automatically when said compressed memory is near full.

17. A method of operating a computer, comprising:
storing uncompressed data;

moving uncompressed data into a data queue;

compressing the data in the data queue;

storing the compressed data in a compressed memory;

monitoring the compression ratio after compressing;

reducing the precision of the uncompressed data moved into the data queue when the compression ratio drops below a predetermined level and the compressed memory is near full.

18. The method of claim 17, wherein the step of reducing the precision of the uncompressed data improves the compression efficiency.

19. The method of claim 17, wherein the step of reducing precision includes truncating data by reducing bits to zero.

20. The method of claim 17, wherein the step of reducing precision includes denormalizing floating point data by shifting data the number of times represented by an exponent component.

21. A processor, comprising:

a load data queue;

a truncate and scale processing unit;

a compression control register with one or more bits to enable an enhanced compression mode; and

a load processing unit configured to (i) transfer data involved in a load instruction to the truncate and scale processing unit prior to storing the data in the store data queue, when the enhanced compression mode is enabled, and to (ii) transfer the data to the store data queue bypassing the truncate and scale processing unit when the enhanced compression mode is not enabled.

22. The processor of claim 21, wherein:

the processor further comprises a convert processing unit; and

the load processing unit is further configured to transfer data involved in a load instruction to the convert processing unit prior to the transferring the data to the

truncate and scale processing unit, when the enhanced compression mode is enabled.

23. The processor of claim 21, wherein the compression control register is writable by software and comprises one or more bits to control truncate and scale operations performed by the truncate and scale processing unit.